IN THE CLAIMS

Please amend the claims as follows:

1. (original) A semiconductor device comprising a thermally and electrically conductive bottom plate on an upper side of which there is a semiconductor element with a first connection region and a second connection region, said regions being coupled to, respectively a first conductor and a second conductor, said semiconductor element being surrounded by an electrically insulating synthetic resin envelope that covers a side face of the bottom plate, which side face is provided with a recess that is filled with a part of the envelope, characterized in that the recess, viewed in cross-section at right angles to an edge of the bottom plate, takes the form of a staircase with at least two steps.

2. (original) A semiconductor device as claimed in Claim 1, wherein the first and the second conductor form an assembly, of which part is coupled to, respectively, the first and the second connection region, which parts are also being surrounded by an electrically insulating synthetic resin envelope.

3. (original) A semiconductor device as claimed in Claim 1, characterized in that the height of the recess at the location of the first step lies in the range between 20 and 60 μm and at the location of the second step in the range between 100 and 150 μm, while the width of the steps ranges between 0.2 and 0.4 mm.

4. (currently amended) A semiconductor device as claimed in Claim 1~~or 2~~, characterized in that the device comprises a further electrically conductive bottom plate that is separated from the bottom plate and on which a further semiconductor element is situated having a first and a second further connection region, said regions being coupled to, respectively a first further conductor and a second further conductor, said further semiconductor element being surrounded by the electrically insulating synthetic resin envelope that is connected to the further bottom plate in a way similar to the manner in which it is connected to the bottom plate.

5. (original) A semiconductor device as claimed in Claim 4, wherein the first and second further conductor are part of the assembly, of which part is coupled to the further semiconductor elements, said part also being surrounded by the resin envelope.

6. (currently amended) A semiconductor device as claimed in Claim 1 ~~or 2~~, characterized in that the semiconductor element comprises a MOSFET transistor.

7. (original) A semiconductor device as claimed in Claim 6, wherein the connection region of the drain of the MOSFET borders on the bottom plate that projects from the envelope and that forms the drain connection, and wherein the connection regions of the source and the gate of the MOSFET are situated on a side of the MOSFET opposite the connection region of the drain, and the frist and the second conductor form, respectively, the source and the gate connection and project from the envelope.

8. (original) A method of manufacturing a semiconductor device, comprising the steps of:

- providing an electrically conductive bottom plate having an upper side and a lower side, and a side face, at which side face a recess is present, with its lower side on a support plate;
- securing a semiconductor element on the upper side of the bottom plate, which semiconductor element is provided with a first connection region and a second connection region;

- providing an assembly of a first conductor and a second conductor, such that a part thereof is coupled to, respectively, the first and the second connection region,
- surrounding the semiconductor element and the parts of the conductors coupled thereto by an electrically insulating synthetic resin envelope, such that it covers also the side face of the bottom plate and that it projects above the support plate in the recess, and
- removing the support plate,

wherein the recess of the bottom plate has or is given the shape of a staircase with at least two steps, when viewed in a direction transverse and perpendicular to the edge of the bottom plate.

9. (original) A method as claimed in Claim 8, wherein the recess is formed by means of a punch technique.

10. (currently amended) A method as claimed in Claim 8 ~~or 9~~, characterized in that the assembly of conductors and the bottom plate is formed from two conductor frames, one of which comprises the bottom plate and a conductor, and the other one of which comprises another conductor, and after securing the semiconductor element to the bottom plate in one conductor frame, the other conductor frame is secured to the semiconductor element, after

which the envelope is provided and superfluous parts of the conductor frames are removed.